US-PAT-NO: 6369855

DOCUMENT-IDENTIFIER: US 6369855 B1

TITLE: Audio and video decoder circuit and system

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US Patent No. - PN (1):
6369855

Brief Summary Text - BSTX (51):
The present invention provides a JTAG interface.

Brief Summary Text - BSTX (74):
It is an object of the present invention to provide a JTAG interface.

Detailed Description Text - DETX (8):
In addition, a JTAG block 280-6 is depicted that allows for testing of this
circuit using a standard JTAG interface that is interconnected with this JTAG
block.

Detailed Description Text - DETX (20):
DES 212 processing is signaled by the arrival of a control word packet.
That is, a conditional access is triggered by the arrival of a control word
packet (CWP). The ARM firmware recognizes a CWP has been received and hands it
to the Verifier, which is NewsDataCom (NDC) application software running on the
ARM 220. The Verifier reads the CWP and communicates with an external Smart
Card through a Smart Card I/O interface in communication coprocessor 280.
After verification, it passes the pointer to an 8 byte key

back to the
firmware, which then loads the key for the DES 212 to decrypt succeeding
packets.

Detailed Description Text - DETX (71):
JTAG boundary scan is included in the circuit 200. Five pins (including a
test reset) are used to implement the IEEE 1149.1 (JTAG) specification. The
port includes an 8-bit instruction register used to select the instruction.
This register is loaded serially via the TDI input. Four instructions (Bypass;
Extest; Intest and Sample) are supported, all others are ignored. Timing for
this interface conforms to the IEEE 1149.1 specification.

Detailed Description Text - DETX (407):
The Communications Co-Processor module 280 provides two programmable timers,
3 UARTs--one for Smart Card and two for general use, accepts IR, SIRCSI and RF
signals and provides a SIRCSO output. It also provides two general purpose
I/Os and manages the I.sup.2 C and JTAG interfaces.

Detailed Description Text - DETX (408):
This module 280 contains a collection of buffers, control registers, and
control logic for various interfaces, such as UARTs, IR/RF, I.sup.2 C, and
JTAG. All the buffers and registers are memory mapped and individually managed
by the ARM CPU 220. Interrupts are used to communicate between these interface
modules and the ARM CPU.

Detailed Description Paragraph Table - DETL (34):
TABLE 25 List of Signal Pins and Their Descriptions

Signal Name	#	I/O	Description
Transport Parser DATAIN[7:0]*	8	I	Data Input. Bit 7 is the first bit in the transport stream
DCLK*	1	I	Data Clock. The

maximum frequency is
7.5 MHz. PACCLK* 1 I Packet Clock. Indicates valid packet
data on DATAIN.
BYTE_STRT* 1 I Byte Start. Indicates the first byte of a
transport packet for
DVB. Tied low for DSS. DERROR* 1 I Data Error, active
high. Indicates an
error in the input data. Tie low if not used. CLK27* 1 I
27 MHz Clock input
from an external VCXO. VCXO_CTRL* 1 O VCXO Control.
Digital pulse output for
external VCXO. CLK_SEL 1 I Clock select. CLK_SEL low
selects a 27 MHz input
clock. When high, selects an 81 MHz input clock.
Communications Processor
IR* 1 I Infra-Red sensor input RF* 1 I RF sensor input
SIRCSI* 1 I SIRCS
control input SIRCSO* 1 O SIRCS control output UARTDI1* 1
I UART Data Input,
port 1 UARTDO1* 1 O UART Data Output, port 1 UARTDI2* 1 I
UART Data Input,
port 2 UARTDO2* 1 O UART Data Output, port 2 PDATA 8 I/O
1394 Interface Data
Bus PWRITE 1 O 1394 Interface Write Signal PREAD 1 O 1394
Interface Read
Signal PPACEN 1 I/O 1394 Interface Packet Data Enable
PREADREQ 1 I 1394
Interface Read Data Request PERROR 1 I/O 1394 Interface
Error Flag IIC_SDA* 1
I/O I.sup.2 C Interface Serial Data IIC_SCL* 1 I/O I.sup.2
C Interface Serial
Clock IO1* 1 I/O General Purpose I/O IO2* 1 I/O General
Purpose I/O
Extension Bus EXTR/W 1 O Extension Bus Read/Write. Selects
read when high,
write when low. EXTWAIT 1 I Extension Bus Wait Request,
active low, open
drain EXTADDR[24:0] 25 O Extension Address bus: byte
address EXTDATA[15:0] 16
I/O Extension Data bus EXTINT[2:0] 3 I External Interrupt
requests (three)
EXTACK[2:0] 3 O External Interrupt acknowledges (three)
CLK40 1 O 40.5 MHz
Clock output for extension bus and 1394 interface CS1 1
O Chip Select 1.
Selects EEPROM, 32M byte maximum size. CS2 1 O Chip
Select 2. Selects
external DRAM. CS3 1 O Chip Select 3. Selects the modem.

CS4 1 O Chip Select
4. Selects the front panel. CS5 1 O Chip Select 5. Selects front end control.
CS6 1 O Chip Select 6. Selects the 1394 interface. CS7 1 O Chip Select 7.
Selects the parallel data port. RAS 1 O DRAM Row Address Strobe UCAS 1 O
DRAM Column address strobe for upper byte LCAS 1 O DRAM Column address strobe
for lower byte SMIO 1 I/O Smart Card Input/Output SMCLK 1 O Smart Card
Output Clock SMCLK2 1 I Smart Card Input Clock, 36.8 MHz SMDETECT 1 I Smart
Card Detect, active low SMRST 1 O Smart Card Reset SMVPPEN 1 O Smart Card Vpp
enable SMVCCDETECT* 1 I Smart Card Vcc detect. Signals whether the Smart
Card Vcc is on. SMVCCEN 1 O Smart Card Vcc enable Audio Interface AUD_PLLI*
1 I Input Clock for Audio PLL AUD_PLLO 1 O Control Voltage for external filter
of Audio PLL PCM_SRC 1 I PCM Clock Source Select. Indicates whether the
PCM clock is input to or generated by the circuit. PCMDATA* 1 O PCM Data
audio output. LRCLK* 1 O Left/Right Clock for output PCM audio data. PCMCLK*
1 I or PCM Clock. O ASCLK* 1 O Audio Serial Data Clock SPDIF* 1 O SPDIF
audio output Digital Video Interface YCOUT[7:0] 8 O 4:2:2 or 4:4:4 digital
video output YCCLK 1 O 27 or 40.5 MHz digital video output clock YCCTRL[1:0]
2 O Digital video output control signal NTSC/PAL Encoder Interface NTSC/PAL
1 I NTSC/PAL select. Selects NTSC output when high, PAL output when low.
SYNCSEL 1 I Sync signal select. When low, selects internal sync generation.
When high, VSYNC and HSYNC are inputs. VSYNC 1 I or Vertical synchronization
signal O HSYNC 1 I or Horizontal synchronization signal O YOUT 1 O Y signal
Output BIASY 1 I Y D/A Bias-capacitor terminal COUT 1 O C signal Output
BIASC 1 I C D/A Bias-capacitor terminal COMPOUT 1 O Composite signal Output
BIASCOMP 1 I Composite Bias-capacitor terminal IREF 1 I

Reference-current
input COMP 1 I Compensation-capacitor terminal VREF 1 I
Voltage reference
SDRAM Interface SDATA[15:0] 16 I/O SDRAM Data bus.
SADDR[11:0] 12 O SDRAM
Address bus. SRAS 1 O SDRAM Row Address Strobe SCAS 1 O
SDRAM Column Address
Strobe SWE 1 O SDRAM Write Enable SDOMU 1 O SDRAM Data
Mask Enable, Upper
byte. SDOML 1 O SDRAM Data Mask Enable, Lower byte. SCLK
1 O SDRAM Clock
SCKE 1 O SDRAM Clock Enable SCS1 1 O SDRAM Chip Select 1
SCS2 1 O SDRAM Chip
Select 2 Device Control: RESET* 1 I Reset, active low
TDI* 1 I JTAG Data
Input. Can be tied high or left floating. TCK* 1 I JTAG
Clock. Must be tied
low for normal operation. TMS* 1 I JTAG Test Mode Select
Can be tied high or
left floating. TRST* 1 I JTAG Test Reset, active low. Must
be tied low or
connected to RESET for normal operations. TDO* 1 O JTAG
Data Output Reserved
3 Reserved for Test VCC / GND 10 Analog supply VCC / GND
44 Digital supply
*indicates a 5 volt tolerant pin

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(12) **United States Patent**
Chauvel et al.

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(54) **AUDIO AND VIDEO DECODER CIRCUIT AND SYSTEM**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Oct. 31, 1997**

Related U.S. Application Data

(60) Provisional application No. 60/030,107, filed on Nov. 1, 1996, provisional application No. 60/030,106, filed on Nov. 1, 1996, provisional application No. 60/030,105, filed on Nov. 1, 1996, provisional application No. 60/030,104, filed on Nov. 1, 1996, provisional application No. 60/030,108, filed on Nov. 1, 1996, and provisional application No. 60/029,923, filed on Nov. 1, 1996.

(51) **Int. Cl.**[7] **H04N 7/26**
(52) **U.S. Cl.** **348/423.1**; 348/558; 370/474
(58) **Field of Search** 370/474; 348/558, 348/553, 423, 461, 569, 564, 423.1

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(57) **ABSTRACT**

An improved audio-visual circuit is provided that includes a transport packet parsing circuit for receiving a transport data packet stream, a CPU circuit for initializing said integrated circuit and for processing portions of said data packet stream, a ROM circuit for storing data, a RAM circuit for storing data, an audio decoder circuit for decoding audio portions of said data packet stream, a video decoder circuit for decoding video portions of said data packet stream, an NTSC/PAL encoding circuit for encoding video portions of said data packet stream, an OSD coprocessor circuit for processing OSD portions of said data packets, a traffic controller circuit moving portions of said data packet stream between portions of said integrated circuit, an extension bus interface circuit, a P1394 interface circuit, a communication coprocessors circuit, an address bus connected to said circuits, and a data bus connected to said circuits.

12 Claims, 76 Drawing Sheets